



# CT43x Design Recommendation

## Description

The objective of this document is to help design engineers implement and use Crocus Technology's new XtremeSense® TMR technology based CT430 and CT431 integrated contact current sensors in their designs. The application note provides circuit and Printed Circuit Board (PCB) layout recommendations, as well as other recommendations and tips.

For additional information and details please contact: [support@crocus-technology.com](mailto:support@crocus-technology.com).

## Summary

The following topics are discussed in this document:

- Package and Pin-out
- Schematic Recommendations
- Layout Recommendations
- Isolation
- Filtering
- Thermal Considerations
- Stray Magnetic Field Reduction
- Reflow Conditions

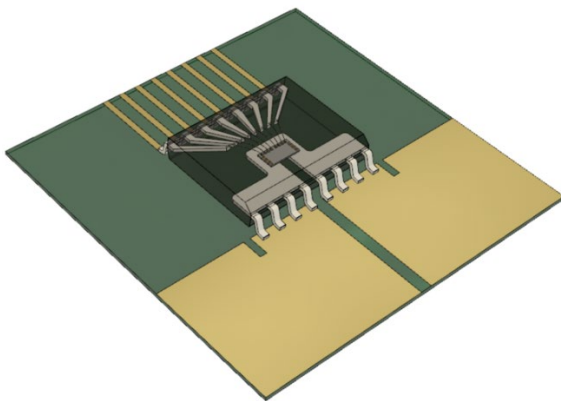


Figure 1. Overview of CT43x in SOICW-16 package on a PCB with a current trace

## Introduction

The CT43x family is a coreless current sensor featuring a 1 MHz bandwidth, 5 kV isolation, stray field magnetic rejection and a total error of less than 1% Full-Scale (FS) over the full -40°C to +125°C operational temperature range.

For the full performance details of the CT43x please refer to AN131.

## Non-ratiometric voltage output

The CT43x is designed to produce the same offset and sensitivity as long as the supply voltage is within the operating range.

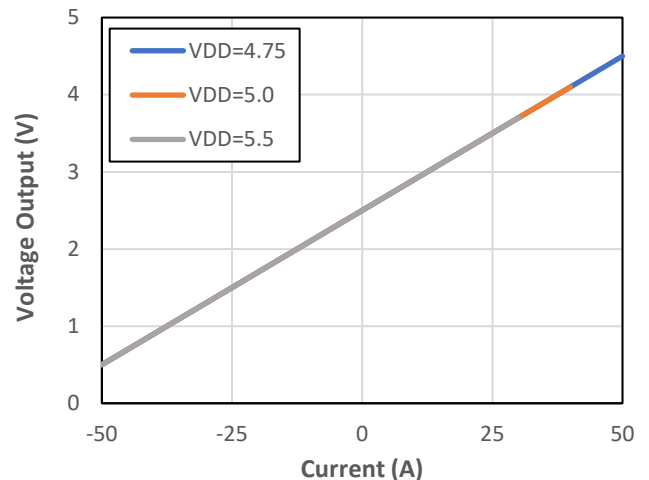


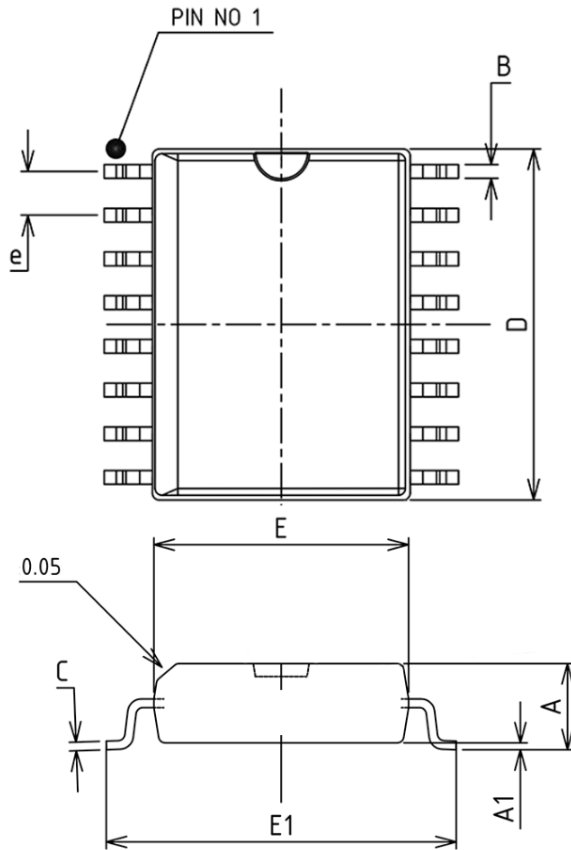
Figure 2. The CT43x output voltage gain and offset do not vary with a varying voltage supply on the VCC pin.

While ratiometry can mitigate some errors when the supply voltage is variable. It cannot be relied upon to provide the high accuracy figures CT43x achieves. Mainly due to ratiometric scaling mismatch. The CT43x with its non-ratiometric design, offers high offset/sensitivity precision, supply voltage noise immunity and design flexibility.



### SOICW-16 package

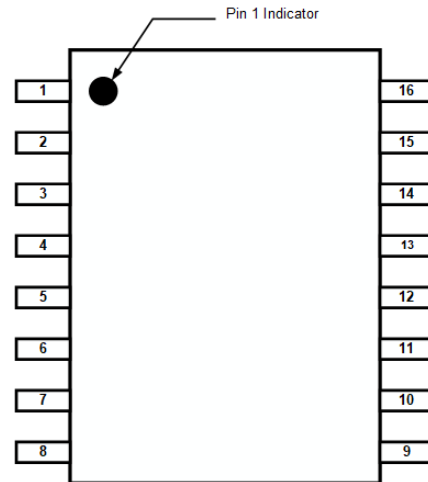
The CT43x is packaged in an industry standard SOICW-16 with a custom internal lead frame. This package offers 9.21 mm and 8.79 mm of creepage and clearance respectively.



Symbol	Dimension (mm)
A	2.540
A1	0.200
B	0.400
C	0.254
D	10.20
E	7.500
E1	10.31
e	1.270

### Pinout

Please refer to the following table for pin name of CT43x:



Pin #	Name	Function
1-4	IP+	Input current
5-8	IP-	Output current
9	VREF	Reference voltage output
10	GND	Ground
11	FLT	Fault detection output
12	FILTER	Helps set a low-pass filter
13	OUT	Voltage output
14	N/C	Do not connect
15	VCC	Supply Voltage
16	N/C	Do not connect

### Schematics Recommendations

#### Decoupling capacitor

A 1  $\mu$ F capacitor located as close as possible to the VDD pin is highly recommended. Decoupling capacitors avoid UVLO in case of a sudden V<sub>DD</sub> drop and provides a relatively cleaner voltage supply free of voltage ripples.

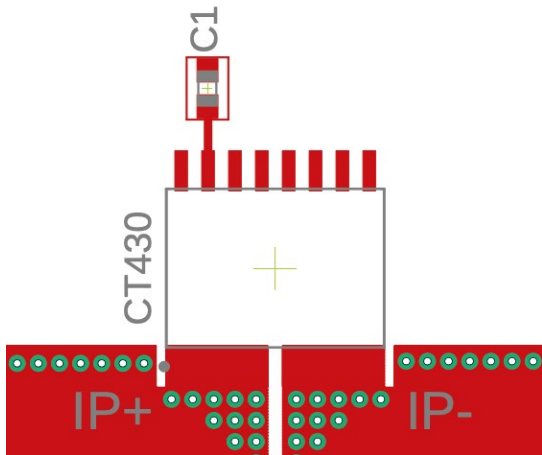


Figure 3. CT43x footprint along with a decoupling capacitor C1.

### Single-Ended ADC

The CT43x features a non-ratiometric voltage output ( $V_{OUT}$ ). The OUT pin can be directly connected to a single-ended ADC input with a precise internal or external voltage reference voltage. Which is typically available in MCU integrated ADCs.

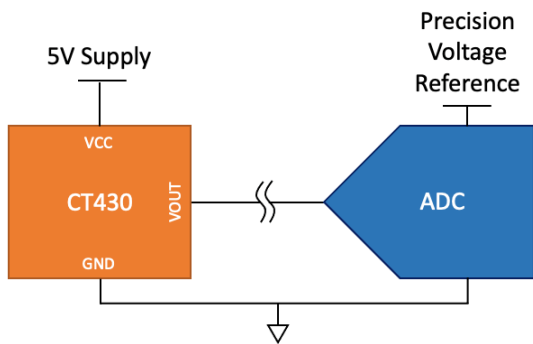


Figure 4. CT43x connected to a single-ended ADC.

### Differential ADC

In noisy environments such as power systems with fast switching transistors, the VREF pin of the CT43x can be used along with the OUT pin to generate a differential voltage that can be used with a differential input ADC. The main benefit of measuring  $V_{REF}-V_{OUT}$  is to mitigate the  $dV/dt$

transients and supply noise that appears on the voltage supply and signal traces.

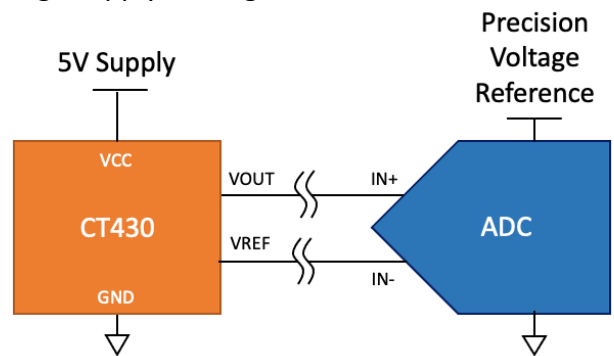


Figure 5. CT43x connected to a differential ADC input.

Contrary to Hall-effect based sensors, VREF is not needed to minimize offset temperature drift on the CT43x.

### Reference Voltage (VREF) Pin

The CT43x's VREF pin is intended to be used as a voltage reference only. Hence, it does not sink/source more than 5 mA. For this reason, a series resistor of 10 kΩ is highly recommended to guarantee the precision of the voltage output.

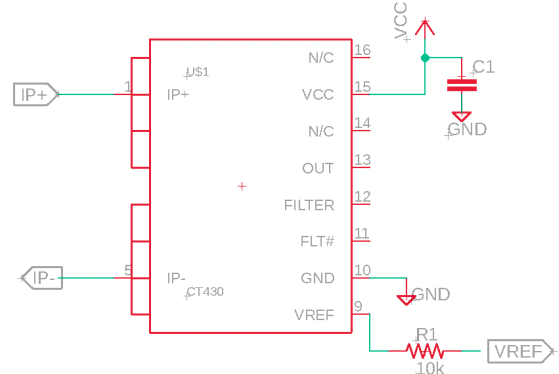


Figure 6. CT43x with a 10 kΩ R1 resistor connected in series to the VREF pin.

### Fault Pin

The FAULT pin is an open-drain output that can sink up to 20 mA. When active, the FAULT pin is pulled low by CT43x, otherwise, it assumes a high-Z value. Depending on the design requirements, a pull-up resistor can be used.

## PCB Layout Recommendation

### Footprint

The recommended footprint for the CT43x is detailed below. Please note that this footprint is able to achieve 8 mm creepage between the pins carrying the primary current (pins 1 to 8) and the signal pins.

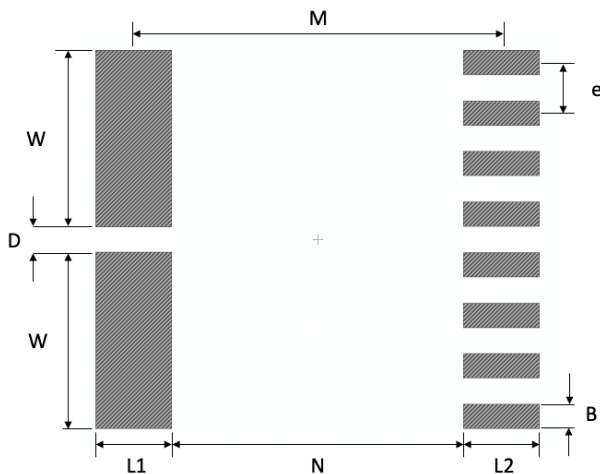


Figure 7. CT43x SOICW-16 recommended footprint.

Symbol	Dimension (mm)
B	0.60
D	0.66
e	1.27
L1	1.70
L2	1.70
M	9.75
N	8.05
W	4.42

### Current Carrying Trace

The current trace design is very important as it impacts different aspects of the overall performance of the current sensing system:

#### 1. Heating

By implementing the recommendations below, the heat generation is minimized:

- Using at least a 70  $\mu\text{m}$  (2 oz) copper thickness
- Using at least a 4-layer board
- Adding thermal-vias close to the primary current pins.

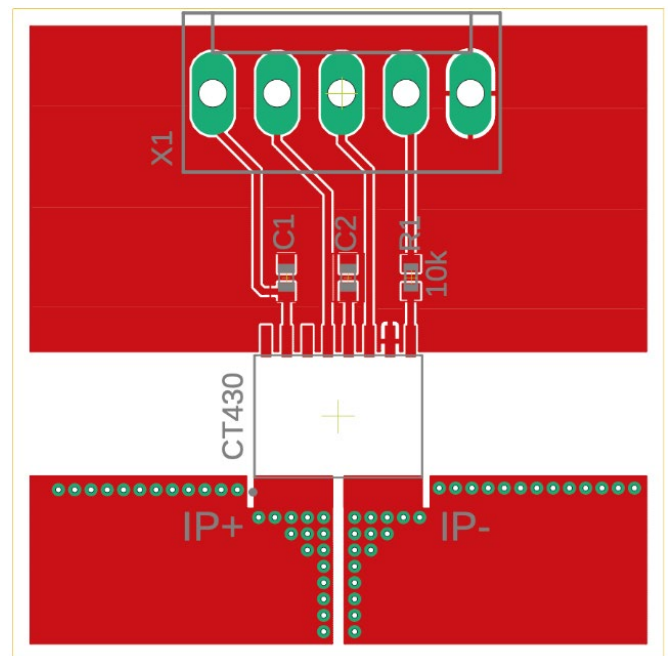


Figure 8. Layout of Current carrying trace and the signal traces.

#### 2. Magnetic Coupling

To reduce any magnetic interference generated by the current trace:

- The orientation of the current traces is important. Ideally, the current traces should not come from behind the sensor.
- The current trace should not be extended below the package.

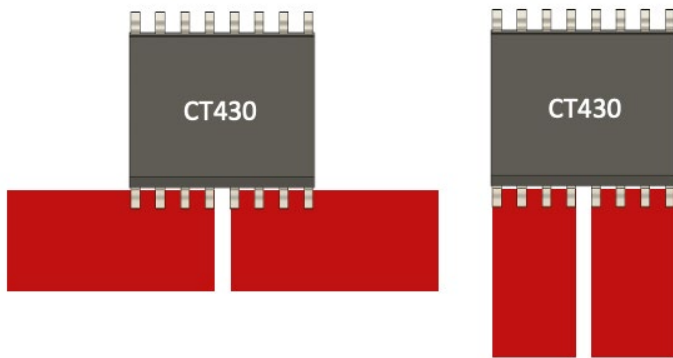


Figure 9. Recommended layouts of the current carrying trace.

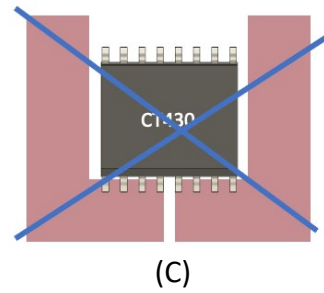


Figure 11. CT43x recommended (b) and not recommended (a) and (c) layouts for isolation.

### Signal Traces

All signal paths on the PCB should be as wide and short as possible to avoid electrical noise from external capacitive coupling. Signal pins are numbered 9 to 16.

### Isolation

The package of the CT43x is compliant with safety standard UL61800-5-1. The clearance and creepage between the primary conductor and the signal paths is more than 8.79 mm and 9.21 mm respectively.

If the creepage is shorter than the design requirement, it is possible to increase it more than 9 mm by adding a slit in the board as shown below.

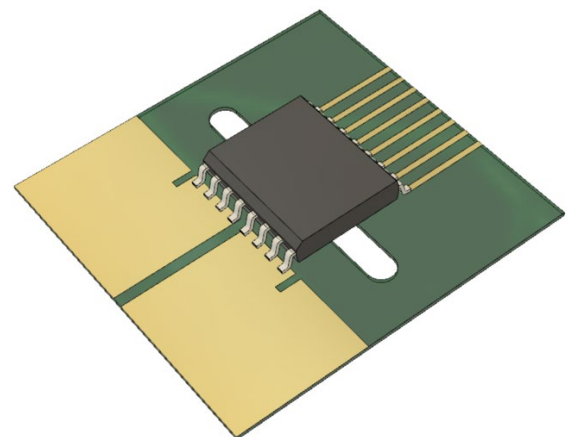


Figure 12. CT43x PCB with a slit to increase creepage.

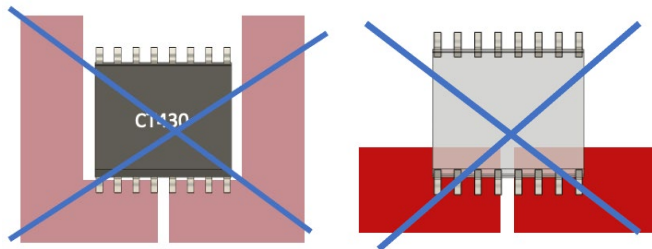
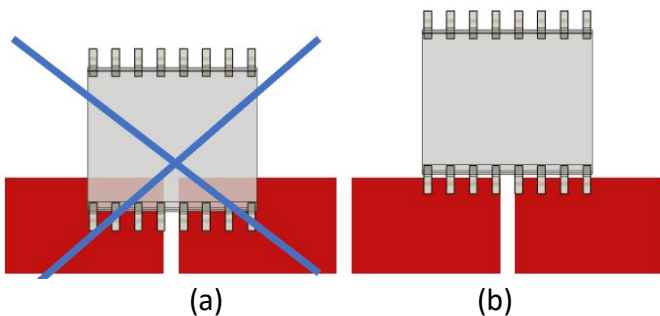


Figure 10. Not recommended.

### 3. Isolation

The distance between the current trace and the signal pins needs to be maximized.

Hence, extending the current trace below the package or behind the sensor leads to shorter distances between the current trace and signal traces reducing the isolation specification.





In terms of safety, the CT43x is certified as IEC/UL 62368-1 and UL1577 compliant.

### Filtering

In applications where the full 1 MHz bandwidth of the CT43x is not required by the design constraints, the filter pin allows the user to implement a low-pass filter that will reduce bandwidth which provides benefits in terms of noise and resolution. A single capacitor is used to implement a low-pass filter thanks to the integrated 15 kΩ resistor already in the chip.

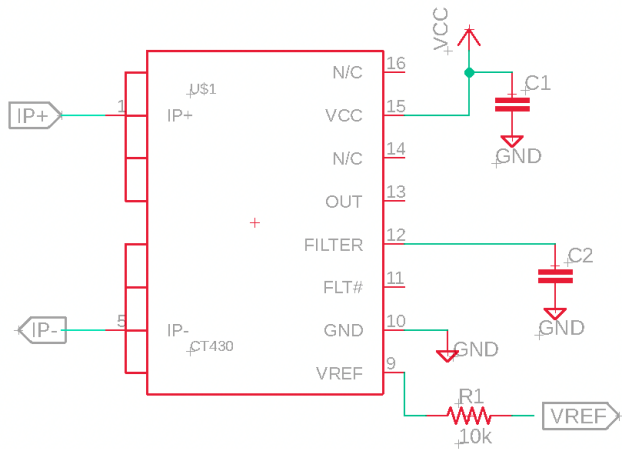


Figure 13. CT43x using the capacitor C2 to implement a low-pass filter.

Below is a table for recommended capacitor values along with the obtained bandwidths.

C (pF)	BW (kHz)	Noise (mA <sub>RMS</sub> )
5	1,000	15
10	500	12
20	250	11
47	100	9

### Thermal Considerations

The CT43x is capable of supporting up to 50 A<sub>RMS</sub> continuous current at room temperature and even larger current for short bursts.

The junction temperature is the limiting factor and needs to stay below +130°C. The main parameters that contribute to the junction temperature are:

- Ambient temperature
- PCB layout and characteristics
- Primary current

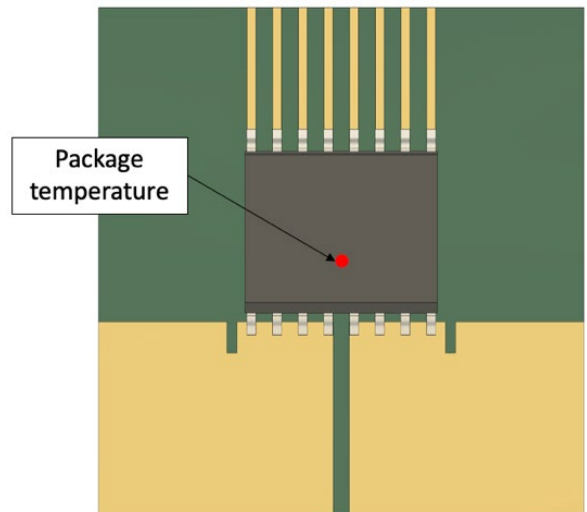


Figure 14. CT43x SOICW-16 with a red dot showing the relative hottest point on the package.

The junction temperature can be estimated by measuring temperature on the red dot shown above.

### Reference measurements

All the measurements below were done using the CT430 (CTD430-50DC) demo board. The figure below shows the rise of junction temperature T<sub>j</sub> relative to the ambient temperature versus continuous current at different ambient temperatures.





### T<sub>j</sub> rise vs Applied Bus-Bar Current

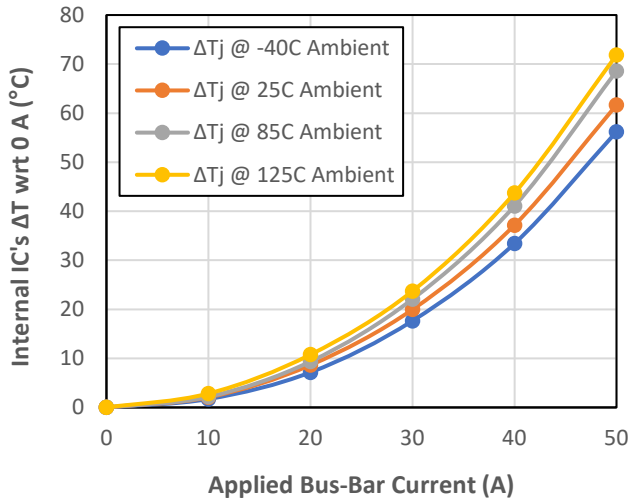


Figure 15. Junction temperature of CT43x vs. applied current through the bus-bar.

The graph below shows the rise in temperature on the package versus time.

### Package Temperature over Time

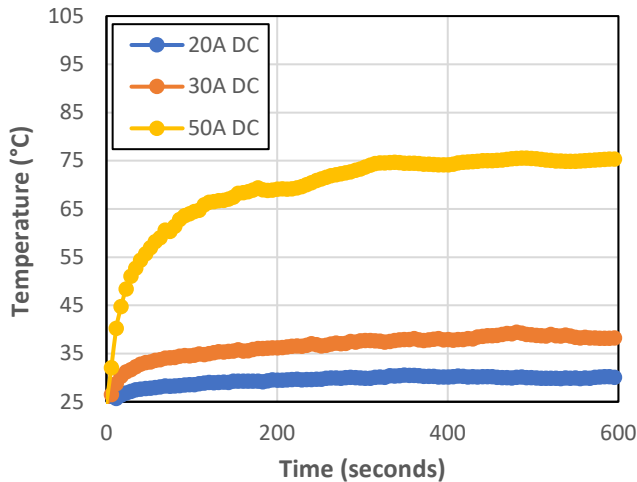


Figure 16. Package temperature of CT43x over time.

### Stray Magnetic Field Reduction

The CT43x benefits from two (2) advantages when it comes to Common Mode Field Rejection (CMFR):

#### Axis of sensitivity

XtremeSense® TMR has a planar axis of sensitivity as opposed to Hall-effect perpendicular orientation of sensitivity. The CT43x is then better suited to handle crosstalk magnetic fields generated by adjacent current carrying conductors. As shown below, the magnetic field generated by a close by conductor is mainly perpendicular.

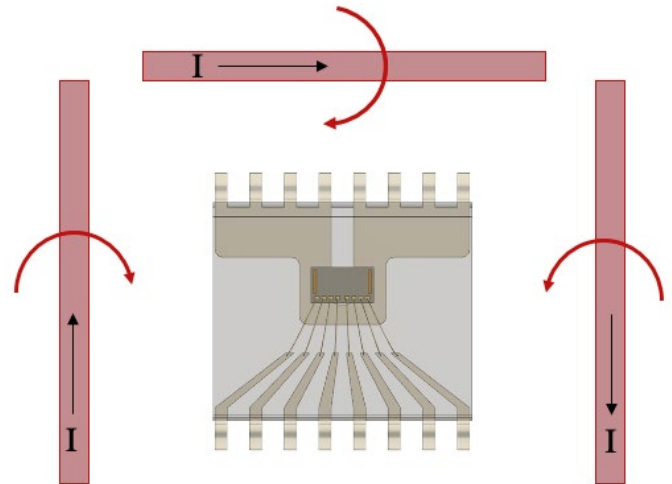


Figure 17. CT43x along with 3 adjacent current carrying conductors pictured in red.

#### Differential Sensing

The CT43x uses two (2) full-bridge XtremeSense® TMR sensors to achieve differential sensing capability which allows CMFR.

A detailed analysis of the CT43x CMFR is available on AN131.

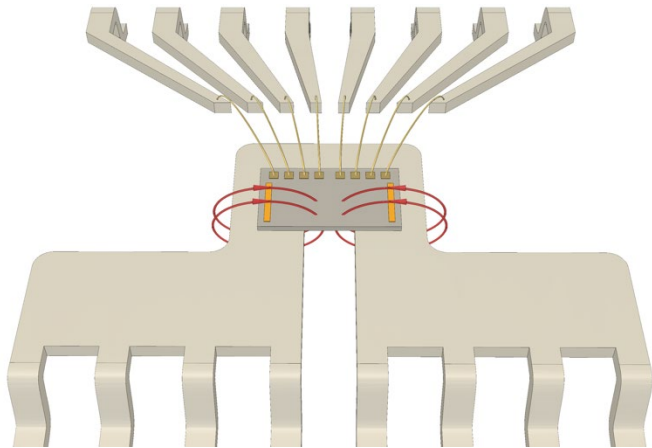


Figure 18. CT43x lead frame approximation showing the internal U-shape that allows differential sensing capability.

The CT43x family is meant to be used in magnetically noisy environments and in designs containing multiple current paths.

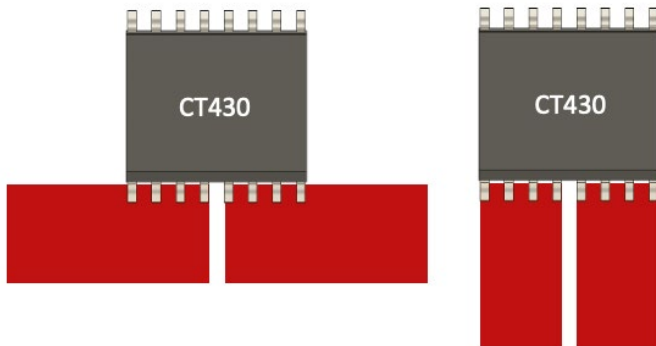


Figure 19. Recommended layouts of the current carrying trace.

## Reflow Conditions

Recommended reflow temperature profile below is outlined in table below and Figure 20. For more details, please see application note AN125 on Crocus' website.

Parameter	1	TC Mean	TC Range
Peak Temperature	261.4°C	261.4°C	0
Rising Temperature Between +150°C to +200°C	87.31 s	87.31 s	0
Total Time above +217°C	69.88 s	69.88 s	0
Total Time above +255°C	36.61 s	36.61 s	0

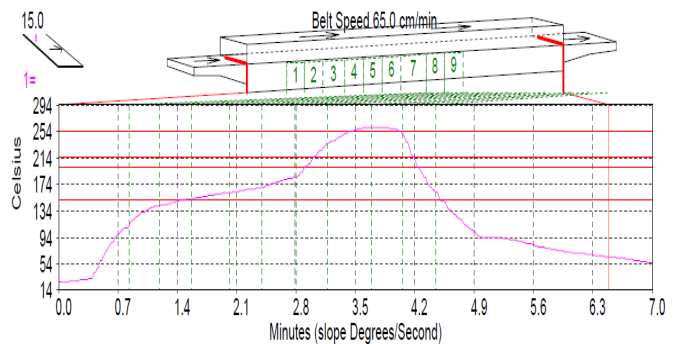


Figure 20. Lead-free solder temperature profile and belt speed for Crocus' products.

## Other Information

Please check our website [www.crocus-technology.com](http://www.crocus-technology.com) for additional documentation or contact [support@crocus-technology.com](mailto:support@crocus-technology.com).